IN THE CLAIMS

The following listing of claims replaces all prior claim versions and listings.

1. (Original) A data processor comprising:

a CPU;

a semiconductor memory device having a precharge duration detector circuit for monitoring a potential on a bit line at the end of a precharge to determine whether or not the potential on the bit line has reached a predetermined potential; and

a control circuit for resetting the operation of said CPU when the potential on the bit line has not reached a predetermined potential.

2. (Original) The data processor according to claim 1, wherein said precharge duration detector circuit comprises:

a plurality of latch circuits each for holding an output signal corresponding to the potential on the bit line associated therewith at the end of the precharge, each said latch circuit switching the output signal based on whether or not the potential on the bit line has reached the predetermined potential at the end of the precharge; and

a logic circuit for operating a logical OR of the output signals from said plurality of latch circuits to deliver the result of the operation as an error detection signal.

3. (Currently Amended) A semiconductor memory device ~~which requires~~requiring a precharge for a bit line when data is read therefrom, comprising:

a precharge duration detector circuit for monitoring a potential on the bit line at the end of a precharge to determine whether or not the potential on the bit line has reached a predetermined potential; and

a control circuit configured to signal a clock signal anomaly when the potential on the bit line has not reached the predetermined potential.

4. (Original) The semiconductor memory device according to claim 3, wherein said precharge duration detector circuit comprises:

a plurality of latch circuits each for holding an output signal corresponding to the potential on the bit line associated therewith at the end of the precharge, each said latch circuit switching the output signal based on whether or not the potential on the bit line has reached the predetermined potential at the end of the precharge; and

a logic circuit for operating a logical OR of the output signals from said plurality of latch circuits to deliver the result of the operation as an error detection signal.

5. (Original) A clock frequency detecting method for use in a data processor which comprises a semiconductor memory device that requires a precharge for each bit line when data is read therefrom, for detecting whether or not an externally applied clock is within a predetermined range of frequency said method comprising the steps of:

monitoring a potential on the bit line at the end of a precharge to determine whether or not the potential on the bit line has reached a predetermined potential; and

resetting the operation of a CPU when the potential on the bit line has not reached a predetermined potential.

6. (Original) The clock frequency detecting method according to claim 5, further comprising the steps of:

holding output signals corresponding to the potentials on the bit lines at the end of the precharge;

operating a logical OR of the held output signals; and

delivering the result of the operation as an error detection signal.